REMARKS

Claims 1, 4, 5, 8-17, 19, 20, 22, 23, 25, 26, 28, 29, 31, 32, 34, 35 and 37-40 are pending in this application. By this Amendment, claims 1, 4, 5, 8-17, 19, 20, 22, 23, 25, 26, 28, 29, 31, 32, 34 and 35 are amended. Claims 37-40 are added. No new matter is added by these amendments. Support for the amendment to claims 1 and 10, and new claims 37-40 can be found at least on page 38, line 4 through page 40, line 12, and Figs. 5, 16 and 17 of Applicant's disclosure. Reconsideration of the application based on the above amendments and the following remarks is respectfully requested.

The courtesies extended to Applicant's representative by Examiners Malek and Ghayour at the interview held December 15, 2008, are appreciated. The reasons presented at the interview as warranting favorable action are incorporated into the remarks below and constitute Applicant's record of the interview.

The Office Action, in paragraph 3, rejects claims 1, 4, 5 and 8-15 under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 6,567,484 to Hirota et al. (hereinafter "Hirota") and U.S. Patent No. 4,672,639 to Tanabe et al. (hereinafter "Tanabe"), and further in view of U.S. Patent No. 4,975,702 to Bazes. Additionally, under 35 U.S.C. §103(a), claims 16, 17 , 19 and 20 are rejected as being unpatentable over Hirota, Tanabe and Bazes, and further in view of U.S. Patent No. 5,517,155 to Yamauchi et al. (hereinafter "Yamauchi"); claims 22 and 23 are rejected as being unpatentable over Hirota, Tanabe and Yamauchi, and further in view of U.S. Patent No. 5,796,360 to Wendelrup; claims 25, 26, 31 and 32 are rejected as being unpatentable over Hirota, Tanabe and Bazes, and further in view of U.S. Patent No. 6,477,181 to Fujimori et al. (hereinafter "Fujimori"); claims 28, 29, 34 and 35 are rejected as being unpatentable over Hirota, Tanabe, Bazes and Fujimori, and further in view of what is asserted to be Applicant's admitted prior art. The Applicant respectfully traverses these rejections.

The Office Action asserts that some permissible combination of the applied prior art references, as enumerated above, teach or would have suggested all of the features rectied in at least independent claims 1 and 10. However, the references, in any combination, do not teach the features of amended claims 1 and 10, as shown above. Specifically, the references do not teach "a clock generation circuit that includes an oscillation circuit and generates the first to N-th clocks, the oscillation circuit comprising: inversion circuits that are connected serially; and buffer circuits, an output of each of the inversion circuits being connected to an input of a corresponding buffer circuit among the buffer circuits, an output of a final-stage inversion circuit among the inversion circuits being connected to an input of an initial stage inversion circuit among the inversion circuits via a feedback line, the inversion circuits being disposed along a first line that is parallel to the feedback line, the buffer circuits being disposed along a second line that is parallel to the feedback line but differs from the first line," as positively recited in amended claims 1 and 10.

Referring to Fig. 16, inversion circuits DCP0 - DCP4 are disposed along a first line LN1 that is parallel to the feedback line FL. Buffer circuits, SCP0 - SCP4, are disposed along a second line LN2 that is also parallel to the feedback line FL. LN2 is different from LN1, as illustrated. This configuration makes it possible to reduce the length of the feedback line FL in direct contrast to a configuration where the inversion circuits, DCP0 - DCP4, and the buffer circuits, SCP0 - SCP4, are all disposed along the same line (serially). Therefore, the parasitic capacitance of the feedback line FL is reduced while equalizing the differences between the multi-phase clocks.

Further, as illustrated in Fig. 16, by disposing the feedback FL line in a region between the inversion circuits, DCP0 - DCP4, and the buffer circuits, SCP0 - SCP4, it is possible to substitute a line connecting the final-stage inversion circuit, DCP4, and the buffer circuit, SCP4, for the feedback line. This prevents a situation in which an excess parasitic

capacitance is added to the output of the final-stage inversion circuit, DCP4, whereby the phase difference between the multi-phase clocks becomes non-uniform.

As illustrated in Figs. 16 and 17, the dummy line DL, DLA0 - DLA3, and DLB0 - DLB3, and the feedback line FL are disposed in a region between the inversion circuits, DCP0 - DCP4, and the buffer circuits, SCP0 - SCP4. This ensures that the parasitic capacitance of the outputs of the inversion circuits, DCP0 - DCP4, can be made equal, whereby the phase difference between the multi-phase clocks can be equalized.

The applied prior art references do not teach, nor would they have suggested the above features.

For at least the above reasons, the applied prior art references cannot reasonably be considered to teach, or to have suggested, the combinations of all of the features recited in at least independent claims 1 and 10. Further, claims 4, 5, 8, 9, 11-17, 19, 20, 22, 23, 25, 26, 28, 29, 31, 32, 34 and 35 would also not have been suggested by the applied prior art references for at least the respective dependence of these claims on allowable independent claims 1 and 10, as well as for the separately patentable subject matter that each of these claims recites.

Accordingly, reconsideration and withdrawal of the rejections of claims 1, 4, 5, 8-17, 19, 20, 22, 23, 25, 26, 28, 29, 31, 32, 34 and 35 under 35 U.S.C. §103(a) as being unpatentable over the combination of applied prior art references are respectfully requested.

In view of the foregoing, it is respectfully submitted that this application is in condition for allowance. Favorable reconsideration and prompt allowance of claims 1, 4, 5, 8-17, 19, 20, 22, 23, 25, 26, 28, 29, 31, 32, 34, 35 and 37-40 are earnestly solicited.

Should the Examiner believe that anything further would be desirable in order to place this application in even better condition for allowance, the Examiner is invited to contact the undersigned at the telephone number set forth below.

Respectfully submitted,

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